

REMARKS

Claims 1 and 3-10 are pending in the above-identified application. Claim 2 has been canceled. Claims 1, 3, 4, 9, and 10 have been elected for prosecution on the merits. Claim 1 is independent.

Information Disclosure Statement

The Information Disclosure Statement filed January 25, 2002 has not been acknowledged by the Examiner as to consideration of the references cited therein. Therefore, the Examiner is respectfully requested to provide Applicants with an initialed PTO-1449 Form, indicating consideration of the Information Disclosure Statement submitted January 25, 2002.

Specification

The title has been amended to be more descriptive.

Claim Rejection - 35 U.S.C. 102(b): Hsieh

Claims 1-3 have been rejected under 35 U.S.C. 102(b) as being anticipated by Hsieh (IBM Technical Disclosure Bulletin). Claim 2 has been canceled. Applicants respectfully traverse this rejection.

Claim 1 has been amended to incorporate the subject matter of original claim 2, but expressed as a structural limitation. A novel feature of the present invention is that the Schottky barrier diode and the contact region of the MOSFET have the same structure. In particular, self-aligned silicide layers are formed on desired positions of the source/drain regions and the gate electrodes of the MOSFET as well as at the region for forming the Schottky barrier. Thus,

claim 1 recites "wherein a Schottky barrier, which is a component of the Schottky barrier diode, is formed of a silicide layer, another silicide layer is formed on source/drain regions and a gate electrode, which are components of the MOS transistor, and both of the silicide layers are layers formed at the same time in self-alignment."

Hsieh discloses a silicide Schottky barrier diode and an NPN transistor formed on a silicon substrate. The NPN transistor of Hsieh is of a different structure than the Schottky barrier diode, and does not include a periphery circuit formed of a MOS transistor and a silicide layer. Thus, Hsieh fails to teach or suggest each and every element of claim 1, as well as its dependent claims. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim Rejection - 35 U.S.C. 102: Horiuchi

Claims 1-3 have been rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (IEEE, hereinafter Horiuchi). Applicants respectfully traverse this rejection.

As mentioned above, in the present invention self-aligned silicide layers are formed on desired positions of the source/drain regions and the gate electrodes of the MOSFET as well as at the region for forming the Schottky barrier. Horiuchi discloses a silicide Schottky barrier diode and a MOSFET formed on a single substrate. However, the MOSFET of Horiuchi is of a different structure than the Schottky barrier diode, the silicide layer on the source/drain regions and a silicide layer on a gate electrode are formed of

different materials, and the MOSFET does not include a silicide layer. Thus, Horiuchi fails to teach or suggest each and every element of claim 1, as well as its dependent claims. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim Rejections – 35 U.S.C. 103: Iwata

Claim 4 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh/Horiuchi in view of Iwata et al. (U.S. Patent 6,255,704, hereinafter Iwata). Applicants respectfully traverse this rejection.

Iwata is relied on for teaching conversion of titanium silicide layer to a C54 crystalline structure. However, Iwata does not disclose a Schottky barrier diode and a MOS transistor formed on a single substrate, and thus does not make up for the above stated deficiencies in either Hsieh or Horiuchi. Thus, at least for this reason, the rejection fails to establish *prima facie* obviousness. Accordingly, Applicants respectfully request that the rejections be withdrawn.

Claim Rejection - 35 U.S.C. 103: Tuttle

Claims 9 and 10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh/Horiuchi in view of Tuttle (U.S. Patent 6,122,494). Applicants respectfully traverse this rejection.

Tuttle is relied on for teaching the claimed IC module or IC card. However, Tuttle also does not disclose a Schottky barrier diode and a MOS transistor formed on a single substrate, and thus does not make up for the above stated deficiencies in either Hsieh or Horiuchi. Thus, at least for this reason, the rejection fails to establish prima facie obviousness. Accordingly, Applicants respectfully request that the rejections be withdrawn.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1-10 is respectfully requested.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicants respectfully petition for a one (1) month extension of time for filing a reply in connection with the present application, and the required fee of \$110.00 is attached hereto.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully Submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By:  #19382

Charles Gorenstein

Reg. No. 29,271

P.O. Box 747

Falls Church, VA 22040-0747

(703) 205-8000

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CG/RWD/sjl/ndb

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claim 2 has been canceled.

The claims have been amended as follows:

1. (Amended) An integrated semiconductor circuit device comprising a diode bridge circuit formed of a Schottky barrier diode and a periphery circuit formed of a MOS transistor which are formed on a single silicon substrate, wherein a Schottky barrier, which is a component of the Schottky barrier diode, is formed of a silicide layer, another silicide layer is formed on source/drain regions and a gate electrode, which are components of the MOS transistor, and both of the silicide layers are layers formed at the same time in self-alignment [is made of a silicide layer].